



UNITED STATES DEPARTMENT OF COMMERCE
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AD

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/276,780	03/25/99	HUTTER	L H-27203

023494 MMC1/0926
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EXAMINER

LUU, C

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 09/26/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/276,780

Applicant(s)

HUTTER ET AL.

Examiner

Chuong A Luu

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 through 11 is/are pending in the application.
- 4a) Of the above claim(s) 6-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 through 5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some * c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received.
 2. ☐ received in Application No. (Series Code / Serial Number) _____.
 3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II (claims 1-5) in Paper No. 6 is acknowledged.

PRIOR ART REJECTIONS

Statutory Basis

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 1 through 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Prengle et al.

Prengle discloses a method of fabricating a BiCMOS integrated circuit comprising the steps: **(1)** forming in a single implantation step a base region of a bipolar transistor (3) and a p-well (24) of an n-channel MOS transistor (5), note column 4 lines 7-30 Figure 3, and forming in a single implantation step a collector contact well of a bipolar transistor and an n-well (20) of a p-channel MOS transistor, note column 4 lines 23-29; **(2)** forming an n-type collector region within a semiconductor substrate (2) of lighter doping, note Figure 1 column 4 line 62; forming a plurality of p-type wells (24), at least one of said plurality of p-type wells forming a base region (69) lying between said collector region and a surface of said semiconductor substrate (2), said base

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region (69) adjoining said collector region and extending to said surface, and at least one of said plurality of p-type wells forming an n-channel MOS well, note Figure 1; forming a plurality of n-type wells (8), at least one of said plurality of n-type wells forming a collector contact well (52) lying between said collector region and said surface of said semiconductor substrate (20), said collector contact well (52) adjoining said collector region and extending to said surface, further said collector contact well lying between said base region (69) and said n-channel MOS well, and at least one of said plurality of n-type wells forming a p-channel MOS well; and forming an emitter region (80) adjoining said base region (69), said emitter region (80) extending to said surface (20) note Figure 1; **(3)** further including the step of implanting p-dopants, note columns 4 and 5 lines 60-65 and 10-15, respectively, into said p-type wells, excluding a portion of said base region (69) adjacent said emitter region (80); **(4)** further including the step of implanting n-type dopants into said n-type wells, note column 10 lines 41-42, and into a portion of said base region, note Figure 2i; **(5)** further including the step of implanting n-type dopants into said n-type wells and into a portion of said base region, note column 10 lines 41-42.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Prengle et al. disclose a method of constructing a BiCMOS integrated circuit.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Chuong Anh Luu
Assistant Examiner

CAL
September 15, 2000



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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